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-- Port_Enable
-- version 2 3/5/2004
library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;
library synplify;
use synplify.attributes.all;

entity Port_Enable is port
(
Port_EnableX  : in std_logic_vector(8 downto 0);
CCM_reset     : in std_logic;

Tx_A          : in std_logic;
break         : in std_logic;
Rx_A          : out std_logic;

Rx1           : in std_logic;
Rx2           : in std_logic;
Rx3           : in std_logic;
Rx4           : in std_logic;
Rx5           : in std_logic;
Rx6           : in std_logic;
Rx7           : in std_logic;
Rx8           : in std_logic;
Rx9           : in std_logic;

Tx1           : out std_logic;
Tx2           : out std_logic;
Tx3           : out std_logic;
Tx4           : out std_logic;
Tx5           : out std_logic;
Tx6           : out std_logic;
Tx7           : out std_logic;
Tx8           : out std_logic;
Tx9           : out std_logic;

Rst1          : out std_logic;
Rst2          : out std_logic;
Rst3          : out std_logic;
Rst4          : out std_logic;
Rst5          : out std_logic;
Rst6          : out std_logic;
Rst7          : out std_logic;
Rst8          : out std_logic;
Rst9          : out std_logic);

end Port_Enable;

architecture rtl of Port_Enable is
attribute syn_radhardlevel of rtl : architecture is "tmr";

begin
    -- fsm register

    Tx1 <= (Tx_A and break) WHEN (Port_EnableX(0) = '1') ELSE '1';
    Tx2 <= (Tx_A and break) WHEN (Port_EnableX(1) = '1') ELSE '1';
    Tx3 <= (Tx_A and break) WHEN (Port_EnableX(2) = '1') ELSE '1';
    Tx4 <= (Tx_A and break) WHEN (Port_EnableX(3) = '1') ELSE '1';
    Tx5 <= (Tx_A and break) WHEN (Port_EnableX(4) = '1') ELSE '1';
    Tx6 <= (Tx_A and break) WHEN (Port_EnableX(5) = '1') ELSE '1';
    Tx7 <= (Tx_A and break) WHEN (Port_EnableX(6) = '1') ELSE '1';
    Tx8 <= (Tx_A and break) WHEN (Port_EnableX(7) = '1') ELSE '1';
    Tx9 <= (Tx_A and break) WHEN (Port_EnableX(8) = '1') ELSE '1';
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Rx_A <= Rx1 when Port_EnableX(8 DOWNTO 0) = "000000001" else
        Rx2 when Port_EnableX(8 DOWNTO 0) = "000000010" else
        Rx3 when Port_EnableX(8 DOWNTO 0) = "000000100" else
        Rx4 when Port_EnableX(8 DOWNTO 0) = "000001000" else
        Rx5 when Port_EnableX(8 DOWNTO 0) = "000010000" else
        Rx6 when Port_EnableX(8 DOWNTO 0) = "000100000" else
        Rx7 when Port_EnableX(8 DOWNTO 0) = "001000000" else
        Rx8 when Port_EnableX(8 DOWNTO 0) = "010000000" else
        Rx9 when Port_EnableX(8 DOWNTO 0) = "100000000" else
        '1';

Rst1 <= CCM_reset WHEN (Port_EnableX(0) = '1') ELSE '1';
Rst2 <= CCM_reset WHEN (Port_EnableX(1) = '1') ELSE '1';
Rst3 <= CCM_reset WHEN (Port_EnableX(2) = '1') ELSE '1';
Rst4 <= CCM_reset WHEN (Port_EnableX(3) = '1') ELSE '1';
Rst5 <= CCM_reset WHEN (Port_EnableX(4) = '1') ELSE '1';
Rst6 <= CCM_reset WHEN (Port_EnableX(5) = '1') ELSE '1';
Rst7 <= CCM_reset WHEN (Port_EnableX(6) = '1') ELSE '1';
Rst8 <= CCM_reset WHEN (Port_EnableX(7) = '1') ELSE '1';
Rst9 <= CCM_reset WHEN (Port_EnableX(8) = '1') ELSE '1';

end rtl;
```